

HB303
Brief Sheet
32 BIT RISC MICRO PROCESSOR

1. Overview

HB303 is a high performance and fully static 32 bit X86 processor with the compatibility of Windows based, Linux and most popular 32 bit RTOS. It also integrates 32 KB write through direct map L1 cache, PCI rev. 2.1 32 bit bus interface at 33 MHz, SDR/DDR/DDR2 DRAM controller, ROM controller, IPC (Internal Peripheral Controllers with DMA and

interrupt timer / counter included), Fast Ethernet MAC and FIFO UART within a single 225 pin BGA package to form a system-on-chip (**SOC**). It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC) to bring about desired performance.

2. Features

● RISC Processor Core

- 6 stage pipeline
- Full 32-bit RISC architecture
- Supports versatile operation systems, including Windows based, Linux, DOS and most popular 32-bit RTOS
- Supports MMU function which includes 32 TLB entries
- Operation frequency up to 300 MHz

● Embedded I / D Separated L1 Cache

- 16K I-Cache, 16K D-Cache
- Supports write through policy
- Snooping mechanism support for data coherence between main memory and cache
- Direct map cache architecture

● SDR / DDR / DDR2 DRAM Control Interface

- Supports 16-bit data bus width
- Support DLL for clock phase auto-adjustion
- Support SDR DRAM memory space up to 128MB & speed up to 166 MHz
- Support DDR / DDRII DRAM memory space up to 256MB & data rate up to 333/266 MHz

● MAC Controller

- Support one-port 10/100 fast Ethernet MAC
- IEEE 802.3u MII interface
- IEEE 802.3x flow control in full-duplex mode
- Descriptor architecture for packet TX/RX

● PCI Control Interface

- Support PCI Rev 2.1 specification
- 32-bit bus interface
- Supports up to 3 external PCI master devices on PCI
- Supports PCI clock at 33 MHz
- Supports 3 individual PCI clock pins
- Provides 4 PCI interrupt channels
- 3.3V I/O

● SPI Interface x1

- Support boot up function from SPI flash

● LPC Interface

- LPC revision 1.0 compliant
- Supports LPC DMA
- Supports serial IRQ
- Supports 8/16/32-bit transfer size
- Supports bus master request in DMA channel 4

● Cardbus interface

- Support one Cardbus interface mixed with PCI bus

● External RTC interface x 1

- Provides a direct interface to external RTC chips

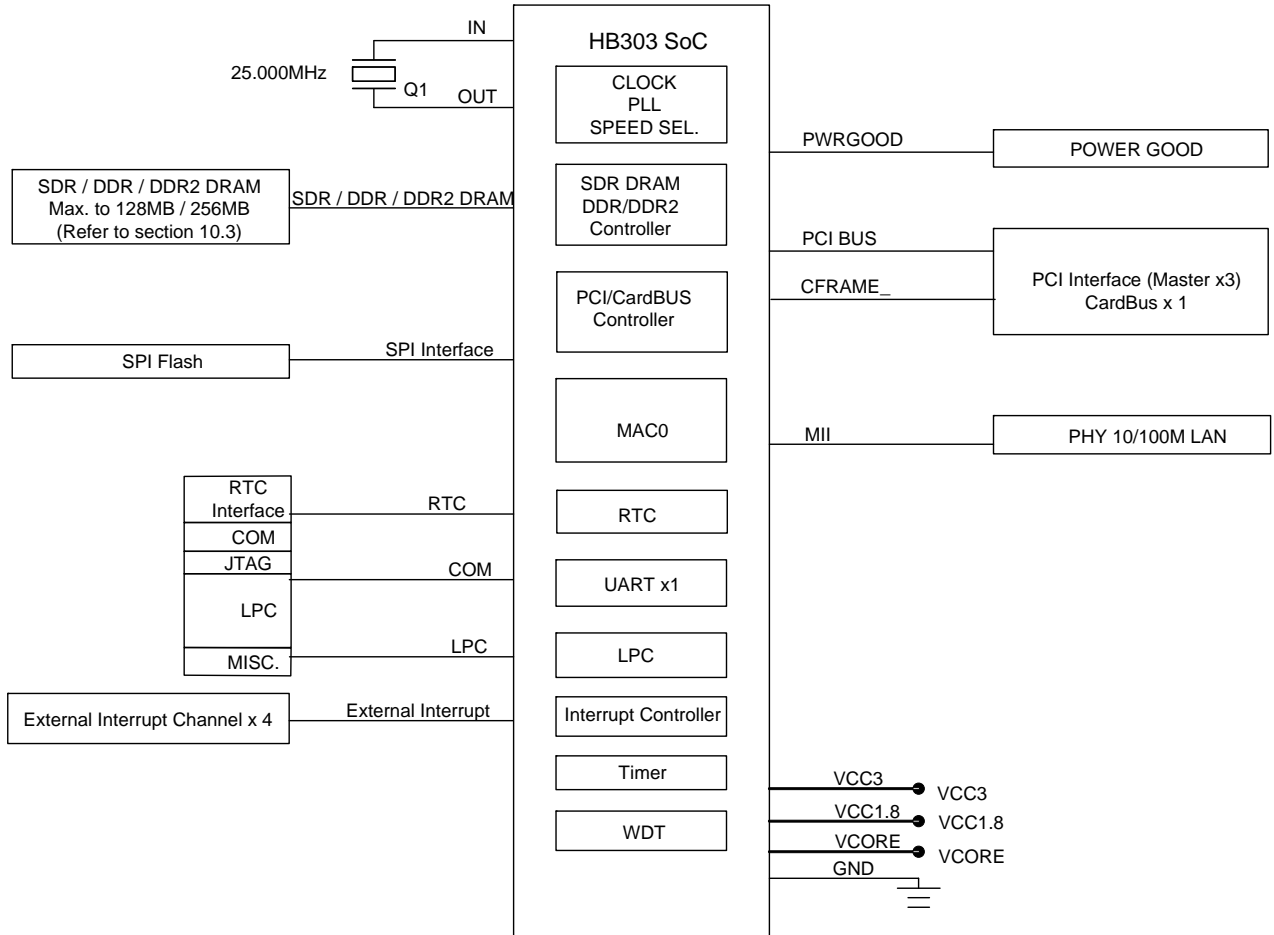
● Interrupt Controller

- Provides two 8259 compatible interrupt controllers which are cascaded internally
- Independent programmable level/edge-triggered interrupt channels

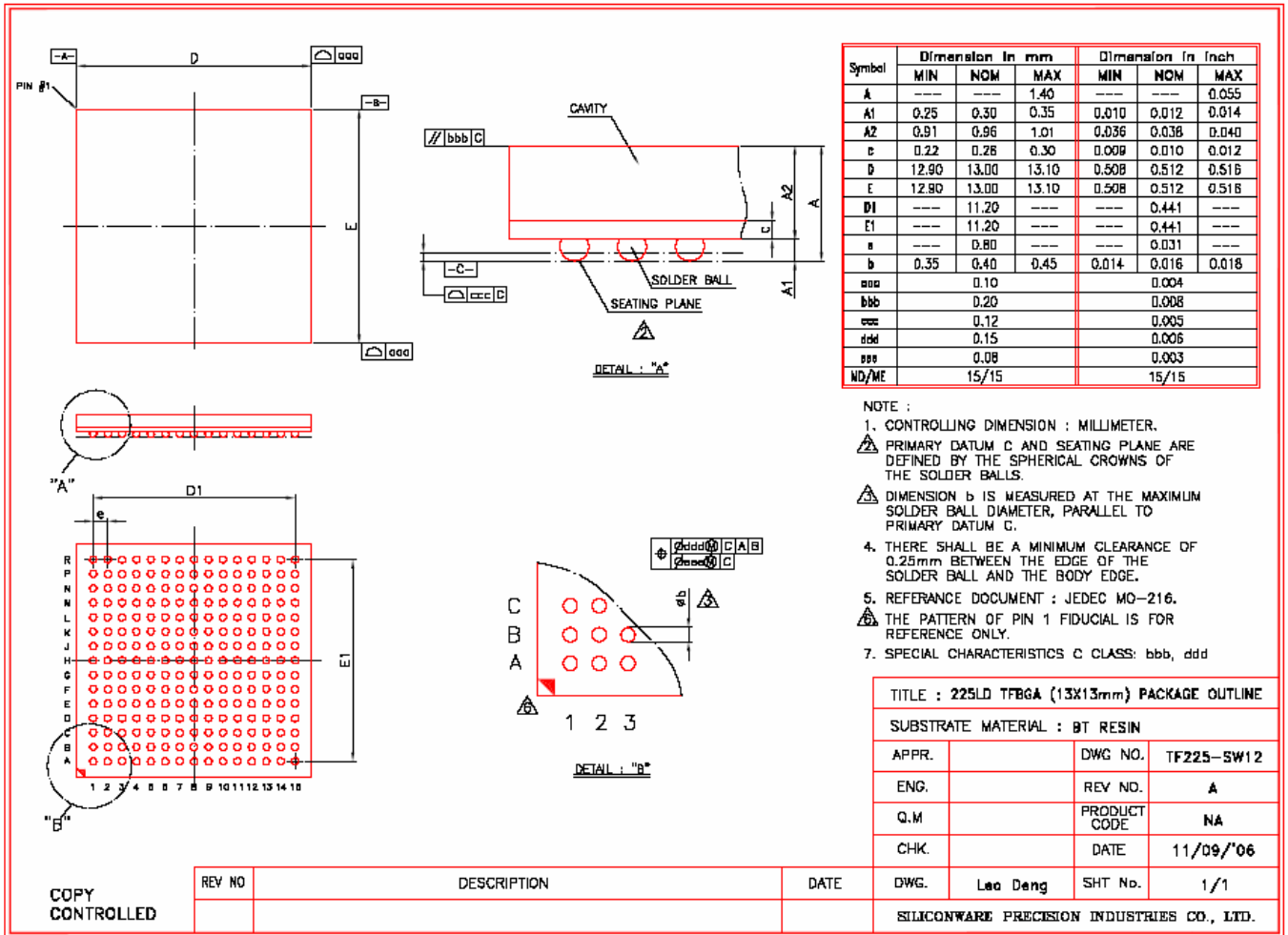
Specifications are subject to change without notice, contact your sales representatives for the most update information.

- **Counter/Timers**
 - 8254 compatible timers
 - Provides three independent programmable timers/counters
 - Supports a watchdog timer(WDT)
- **FIFO UART Port x 1 (1 set COM Port)**
 - Supports the programmable baud rate generator with the data rate from 50 to 460.8K bps
 - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
- **JTAG Interface supported for S.W. debugging**
- **Input clock**
 - 25 MHz
- **Output clock**
 - 25 MHz
 - 33 MHz
 - 100 / 133 / 166 MHz
- **Operating Voltage Range**
 - Core voltage : 1.2 V ~ 1.4 V
 - I / O voltage : 1.8V ± 5% , 3.3 V ± 10 %
- **Package Type**
 - 13 mm x 13 mm, 225 Ball TFBGA
- **Operating temperature :** 0 ~ 70 °C

3. Block Diagram



4. Package Information



REV.B

dl-6700-10